a stress cushioning layer installed on said semiconductor elements,

a lead wire portion extending from said electrode pad to a top of said stress cushioning layer through an opening formed in said stress cushioning layer on said electrode pad,

external electrodes arranged on said lead wire portion on top of said stress cushioning layer, and

a conductor protective layer installed on said stress cushioning layer excluding said external electrodes arranged on said lead wire portion,

wherein said stress cushioning layer, said lead wire portion, said conductor protective layer, and said external electrodes have means for forming each end face on an end surface of said semiconductor elements inside said cutting scribe line and exposing a range from said end face on said end surface of said semiconductor elements to an inside of said cutting scribe line, such that said stress cushioning layer, said lead wire portion, said conductor protective layer, and said external electrodes are located inside of a peripheral edge of said semiconductor elements.

2. (Previously Amended) A semiconductor device according to Claim 1, wherein said end face of said conductor protective layer is formed inside said end face of said stress cushioning layer.

3. (Previously Amended) A semiconductor device according to Claim 1, wherein said end face of said conductor protective layer is formed outside said end face of said stress cushioning layer.

4. (Previously Amended) A semiconductor device according to any one of Claims 1, 2, and 3, wherein an end area of said stress cushioning layer is formed so as

to become tapered and thinner toward said end face of said stress cushioning layer.

5. (Currently Amended) A semiconductor device comprising:

semiconductor elements obtained by cutting a semiconductor wafer having an integrated circuit and an electrode pad formed on one side along a cutting scribe line,

a semiconductor element protective layer installed on said semiconductor elements,

a stress cushioning layer installed on said semiconductor element protective layer,

a first opening formed in said semiconductor element protective layer on said electrode pad,

a second opening formed in said stress cushioning layer on said electrode pad,

a lead wire portion extending to a top of said stress cushioning layer through said first opening and said second opening respectively from said electrode pad,

external electrodes arranged on said lead wire portion on top of said stress cushioning layer, and

a conductor protective layer installed on said stress cushioning layer excluding said external electrodes arranged on said lead wire portion,

wherein said semiconductor element protective layer, said stress cushioning layer, said lead wire portion, said conductor protective layer, and said external electrodes have means for forming each end face on an end surface of said semiconductor elements inside said cutting scribe line and exposing a range from said end face on said end surface of said semiconductor elements to an inside of said cutting scribe line, such that said semiconductor element protective layer, said stress cushioning layer, said lead wire portion, said conductor protective layer, and said external electrodes are located inside of a peripheral edge of said semiconductor elements.

6. (Previously Amended) A semiconductor device according to Claim 5, wherein said end face of said conductor protective layer is formed inside said end face of said stress cushioning layer.

7. (Previously Amended) A semiconductor device according to Claim 5, wherein said end face of said conductor protective layer is formed outside said end face of said stress cushioning layer.

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8. (Previously Amended) A semiconductor device according to Claim 6 or Claim 7, wherein said end face of said semiconductor element protective layer is formed outside said end face of said stress cushioning layer.

9. (Previously Amended) A semiconductor device according to Claim 6 or Claim 7, wherein said end face of said semiconductor element protective layer is formed inside said end face of said stress cushioning layer.

10. (Previously Amended) A semiconductor device according to any one of Claims 5, 6, and 7, wherein an end area of said stress cushioning layer is formed so as to become tapered and thinner toward said end face of said stress cushioning layer.

28. (Previously Added) A semiconductor device according to Claim 1, wherein said stress cushioning layer is comprised of a pasty polyimide material.

29. (Previously Added) A semiconductor device according Claim 1,

wherein said stress cushioning layer is made of a low elastomeric material selected from one of fluororubber, silicone rubber, silicon fluoride rubber, acrylic rubber, silicone fluoride rubber, acrylic rubber, hydrogenated nitride rubber, ethylene propylene rubber, chlorosulfonated polystyrene, epichlorohydrin rubber, butyl rubber, urethane rubber, polycarbonate/acrylonitrile butadiene styrene alloy, polysiloxane dimethyl terephthalate/polyethylene terephthalate copolymer polybutylene terephthalate/polycarbonate alloy, polytetrafluoroethylene, fluorinated ethylene propylene, polyarylate, polyamide/acrylonitrile butadiene styrene alloy, denatured epoxy, denatured polyolefin, and siloxane detnatured polyamide-imide.

30. (Previously Added) A semiconductor device according to Claim 5, wherein said stress cushioning layer is comprised of a pasty polyimide material.

31. (Previously Added) A semiconductor device according Claim 5, wherein said stress cushioning layer is made of a low elastomeric material selected from one of fluororubber, silicone rubber, silicon fluoride rubber, acrylic rubber, silicone fluoride rubber, acrylic rubber, hydrogenated nitride rubber, ethylene propylene rubber, chlorosulfonated polystyrene, epichlorohydrin rubber, butyl rubber, urethane rubber, polycarbonate/acrylonitrile butadiene styrene alloy, polysiloxane dimethyl terephthalate/polyethylene terephthalate copolymer polybutylene terephthalate/polycarbonate alloy, polytetrafluoroethylene, fluorinated ethylene propylene, polyarylate, polyamide/acrylonitrile butadiene styrene alloy, denatured epoxy, denatured polyolefin, and siloxane detnatured polyamide-imide.

32. (Previously Added) A semiconductor device according to Claim 5,

wherein said semiconductor element protective layer is made of a material selected from one of polyimide, polycarbonate, polyester, polytetrafluoroethylene, polyethylene, polypropylene, polyvinylidene fluoride, cellulose acetate, polysulfone, polyacrylonitrile, polyamide, polyamide-imide, epoxy, maleic-imide, phenol, cyanate, polyolefin, and polyurethane.

33. (Currently Amended) A semiconductor device, comprising:

at least one semiconductor element including an electrode pad formed on one side along a cutting scribe line;

a stress cushioning layer formed on said semiconductor element;

a lead wire portion extending from said electrode pad to a top of said stress cushioning layer through an opening formed in said stress cushioning layer on said electrode pad;

external electrodes installed on said lead wire portion on top of said stress cushioning layer; and

a conductor protective layer installed on said stress cushioning layer excluding said external electrodes arranged on said lead wire portion,

wherein each end face of said stress cushioning layer, ~~said lead wire portion, and~~ said conductor protective layer~~, and said external electrodes include means for forming each end face~~ is formed on an end surface of said semiconductor element so as to be positioned inside said cutting scribe line and ~~exposing~~to be exposed within a range from said end face on said end surface of said semiconductor ~~element~~element to an inside of said cutting scribe line.

34. (Previously Added) A semiconductor device according to Claim 33, wherein said end face of said conductor protective layer is formed inside said end face of said stress cushioning layer.

35. (Previously Added) A semiconductor device according to Claim 33, wherein said end face of said conductor protective layer is formed outside said end face of said stress cushioning layer.

36. (Previously Added) A semiconductor device according to Claim 33, wherein an end area of said stress cushioning layer is formed so as to become tapered toward said end face of said stress cushioning layer.